REMARKS

Examiner B. Tran is thanked for his thorough examination of the Prior Art, claims 3, 6, 9, 11, 14-15, 18, 22, 24 and 26 have been amended in order to remove objections that have been raised by the Examiner.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

The invention teaches a new method of filling gaps in a plane of and between a pattern of interconnect lines forming a wiring structure on a semiconductor substrate. A network of interconnect lines has been created on a surface of a substrate whereby the interconnect lines are separated by spacings thereby leaving the surface of the substrate exposed between the interconnect lines. A first layer of dielectric is deposited over the interconnect lines including the exposed surface of the semiconductor substrate. An etch back of the first layer of dielectric is performed leaving the first layer of dielectric in place across the bottom of the spacings between the interconnect lines and partially over the top surface of the interconnect lines. A second layer of dielectric is deposited over the etched

back first layer of dielectric. The second layer of dielectric is etched thereby creating exposed portions of the first layer of dielectric while leaving spacers containing the second dielectric on the upper portions of the sidewalls of the interconnect lines. A layer of oxide is deposited over the etched second layer of dielectric thereby including the exposed portions of the first layer of dielectric.

Claim rejections - 35 U.S.C. 103(a)

1) Reconsideration of the rejection of claim 1-5, 8, and 11-15 under 35 U.S.C 103(a) as being unpatentable over Nichols et al. (US 5,602,055) in view of Lee (US 5,663,092) is respectfully requested based on the following arguments.

The process of Nichols et al. (US 5,602,055) creates a contact hole that is formed in a dielectric layer and that extends downwards over respectively laterally adjacent portions of doped polysilicon and the underlying silicon substrate. The key and basic difference therefore between Nichols et al. (US 5,602,055) and the present invention is that Nichols et al. (US 5,602,055) addresses the formation of a contact hole while the present invention addresses the formation of a layer of Inter-

Metal Dielectric (IMD) of uniform density between interconnect lines of polysilicon.

The processing steps of Nichols et al. are compared below on a step for step basis with the processing steps of the invention. Both sequences of processing steps start with the existence of a pattern of interconnect lines. Fig. 2 of Reference 28 is used as a basis for the comparison.

1) Nichols et al. first create a layer of gate oxide underlying the interconnect lines, the interconnect lines of Nichols et al. serve as gate electrodes which are structures that typically require a layer of gate oxide between the gate electrode structure and the underlying substrate for purposes of stress relieve. The process of the invention does not provide for this layer of gate oxide since gate oxide is typically not required between interconnect lines and the underlying substrate

2) Nichols et al. deposit a first layer of dielectric over the wiring structure. This first layer of dielectric is a thin layer of silicon nitride (preferably from 200 to 1000 Angstrom thick and more preferably 400 Angstrom thick) that overlays the sidewalls and bottom of the openings between the wire structure in addition to the surface of the wire structure. Nichols et al. form self-aligned impurity implants thereby creating regions of

different conductivity adjacent to the gate electrodes that form source and drain regions for the gate electrode. The invention does not perform any impurity implants. The invention deposits a first layer of dielectric whereby this layer of dielectric preferably contains High Density Plasma oxide while this first layer of dielectric is not limited in thickness to being a thin layer of dielectric but is in fact a layer of dielectric that substantially fills the openings between the interconnect lines. The invention further etches this first layer of dielectric thereby leaving deposits of the first layer of dielectric in place on the bottom of the openings between the interconnect lines in addition to partially overlaying the surface of the interconnect lines

3) Nichols et al. deposit a second layer of dielectric and etches that second layer of dielectric thereby forming spacers on the sidewalls of the interconnect lines. Nichols et al. are silent about the materials to be used for this second layer of dielectric. The invention deposits a second layer of dielectric (preferably containing PE SiN) and etches this second layer of dielectric thereby forming spacers on only the exposed, upper portions of the sidewalls of the interconnect lines since the lower portions of the interconnect lines are covered with the remains of the first layer of dielectric

4) Nichols et al. deposit a third layer of dielectric and etch this third layer of dielectric to form contact holes through this third layer of dielectric with the previously created source or drain regions of the gate electrode. Nichols et al. are silent about the materials to be used for this third layer of dielectric. The invention deposits a third layer of dielectric which serves as a layer of Inter Metal Dielectric for the pattern of interconnect lines, the third layer of the invention preferably to contain PE TEOS or PE oxide. This third layer of dielectric of the invention is not etched and is not used for the creation of contact holes to underlying regions of different conductivity source as source/drain regions of a gate electrode.

5) Nichols et al. further vary the use of the first layer of dielectric (silicon nitride) in order to either protect the first layer of dielectric by depositing either a second layer of silicon nitride or by varying the sequence in which the second layer of silicon nitride is deposited. This to create a better opening in the third layer of dielectric for better contact establishment with the underlying regions of different conductivity

6) Nichols et al. fill the opening that has been created in the third layer of dielectric with a conducting material thereby creation an electrical contact on the surface of the third layer

of dielectric. The invention does not create any points of electric contact within the scope of the invention.

Where therefore the Nichols et al. invention is aimed at selectively creating contact openings and filling the contact opening with a conductive material including the use of a refractory metal contact, the present invention eliminates the formation of intra-space irregularities or keyholes within the Intra-Metal Dielectric (IMD) of a pattern of conducting lines. The present invention provides, by means of the sequence of processing steps that have been detailed above, a unique profile made up of etched layers of a first and a second dielectric. Over this unique profile a layer of PE TEOS or PE-oxide is deposited which forms a layer of Inter Metal Dielectric that is free of any internal non-uniform distribution of the deposited oxide. Keyholes and the like are therefore eliminated by the process of the invention for forming a layer of IMD.

The second dielectric layer that under Nichols et al. (US 5,602,055) covers the first dielectric layer is a layer that is deposited for the protection and shielding of the underlying layer of conducting material. The present invention does not provide for such a layer and is therefore in this respect different for Nichols et al. (US 5,602,055).

The basic and fundamental difference between the methods of Nichols et al. (US 5,602,055) and the present invention is further emphasized by the facts that Nichols et al. (US 5,602,055) do not disclose the step of etching back a first layer of dielectric or that the first wiring structure contains a lower layer of polysilicon and an upper layer of silicon nitride or that the second dielectric layer further covers the surface of the partially exposed top corners of the wiring structure or that the dielectric material is deposited over the spacers and also over the exposed top corner of the wiring structure, or the step of planarizing the deposited layer of PE-oxide down to the plane of the top surface.

Lee (US 5,663,092) provides a method for creating DRAM cells whereby the conventional problem of misalignment for overlying masks and exposures is eliminated. The Lee (US 5,663,092) method can be applied for openings that must be created for contact holes that are deep and narrow openings where, when using conventional methods of creation for these contact holes, small misalignments can have severe impact in for instance creating shorts between a bit line or a word line and an adjacent storage contact resulting in electrical shorts within the DRAM device. The various layers of material that are

used by Lee (US 5,663,092), among which is a layer of polysilicon, are the conventional materials that are used to create gate electrodes. The wiring structure that Lee (US 5,663,092) addresses are the typical wiring contacts of DRAM devices such as word lines, bit lines, gate electrode contacts and source/drain region contacts. The Lee (US 5,663,092) invention does not address the formation of an IMD layer of the present invention. Lee (US 5,663,092) makes us of different etch rates that apply to different layers of materials. Lee (US 5,663,092) uses a capped gate line and a capped channel line both capped lines preferably containing silicon nitride whereby both types of capped lines are separated by a first dielectric whereby furthermore a second dielectric overlays the capped regions. It is clear that, by proper selection of etch parameters and conditions, the first and second layers of dielectric can be etched at different etch rates than the capped silicon nitride lines thereby deeply penetrating the first and second layers of dielectric for the formation of contact openings that are self-aligned with the capped lines. In this processing sequence any problems of alignment between the capped lines and the contact holes are eliminated due to the self-aligned nature of the etch that is applied for the creation of the contact holes. It must in this be emphasized that the process of the present invention is very specific in its use of

materials and processes to etch these materials in order to achieve the desired objectives. The present invention provides for first depositing a layer of High Density Plasma oxide (HDP oxide) that is etched, forming the beginning of a support structure for the subsequent deposition of a layer of Plasma Enhanced SiN (PE SiN) which is etched. The combined profile of the unetched or remaining HDP-oxide with the unetched or remaining PE SiN provides a profile such that the deposition of a layer of IMD such as PE-TEOS or PE-oxide over this profile results in a uniform deposition of the layer of IMD, whereby this uniformity is specifically provided for the IMD that is deposited between the conducting lines of polysilicon. The present invention therefore is very specific in the selection of materials that can be used for the methods of the invention whereby specifically a layer of PE-TEOS or PE-oxide is selected for the IMD material that is deposited over the created spacers since these materials have not previously and uniquely been identified for this purpose and since these materials are the selected and precise materials that provide a layer of IMD, over the profile of the underlying materials, that allows the invention to achieve its objectives.

It must further be noted that where there may be commonality in materials applied or inferred between Nichols et

al. (US 5,602,055) and the present invention, this commonality of materials is not germane to the differences that exist between Nichols et al. (US 5,602,055) and the present invention.

2. Reconsideration of the rejection of claim 6-7, 16-21, 24 and 26 under 35 U.S.C 103(a) as being unpatentable over Nichols and Lee, and further in view of Jeng et al. (US 5,683,922) is respectfully requested based on the following arguments.

The methods and processes that are provide by Jeng et al. (US 5,683,922) are applied to the formation of self-aligned contacts for the creation of DRAM devices. While Jeng et al. discloses a wet-etching using 20:1 BEO, this etch is however applied to a layer of BPSG and has as objective to partially create contact openings for DRAM source/drain regions. The BEO etch of the invention is applied to a layer of HDP-oxide to thereby partially create an underlying profiles that can be used to successfully deposit a layer of IMD. Therefore, the application of the BEO etch of the invention differ from Jeng et al.

In selecting a specific etchant ratio in the BEO solution, this etchant ration is basic to and selected for the process of the invention in order to achieve the desired profile for the

underlying layers over which the layer of IMD will be deposited. This etchant ration is not arbitrary and has been experimentally derived for best application of the process of the invention.

Claim 26 of the present invention further specifies the planarization of the deposited layer of PE-TEOS or PE-oxide to further emphasize that the method of the invention has provided a layer of IMD that has uniform internal structure and that therefore uniquely lends itself to planarization without further concern for the appearance of irregular surface conditions such as potentially can be caused by key-holes or other irregularities that are internal to the layer of IMD.

3. Reconsideration of the rejection of claim 9 under 35 U.S.C 103(a) as being unpatentable over Nichols and Lee, as applied to claim 1 and further in view of Liaw (US 5,807,779) and rejection of claim 22 under 35 U.S.C 103(a) as being unpatentable over Nichols, Lee and Jeng, as applied to claim 16 is respectfully requested based on the following arguments.

Nichols and Lee are silent about using PECVD to deposit a layer of silicon nitride to a thickness of about 1000 to 2000 Angstrom at a temperature of 400 degrees C.

Liaw teaches the deposition of a layer of silicon nitride using PECVD to a thickness of about 1000 Angstrom, the deposition of silicon nitride as provided by Liaw however provides for a layer of silicon nitride that serves as protective layer for the creation of self-aligned contact areas for DRAM devices and as such is deposited over a surface of gate electrodes. The application of the silicon nitride layer of Liaw is therefore at variance with the application of the layer of silicon nitride of the invention, since the layer of silicon nitride of the invention serves purposes that are at variance with the layer of silicon nitride of Liaw, it is considered required that the layer of silicon nitride of the invention is detailed in order to understand and specify thickness and the like silicon nitride layer properties.

4. Reconsideration of the rejection of claim 10, 13 under 35 U.S.C 103(a) as being unpatentable over Nichols and Lee, as applied to claim 1 and further in view of Kasai (US 5,821,594) and rejection of claim 23, 25 under 35 U.S.C 103(a) as being unpatentable over Nichols, Lee and Jeng, as applied to claim 16, and further in view of Kasai (US 5,821,594) is respectfully requested based on the following arguments.

The specific deposition of a layer of Al_3O_3 for the second layer of dielectric and the specific processing conditions that apply for the deposition of this layer of dielectric are conditions of material and application that apply to the processes of the invention. It has been found that the material Al_3O_3 is particularly suited to be used as a second layer of dielectric of the invention, the processing conditions under which this second layer of dielectric is created are the optimum conditions for the processing conditions of the invention.

Kasai discloses dielectric layers that may be selected from a group containing silicon nitride, silicon nitride oxide and alumina whereby Kasai further discloses the use of CHF_3 as an etchant for these dielectric materials. A layer of protective insulation layers may contain the above indicated materials, which does however not necessarily indicate that a particular material is best suited for a particular application. For this reason, since Al_3O_3 is best suited for the application of the invention, this material has here been specifically identified.

Where claims 13 and 25 specify specific value of etchant gas flow and other processing condition, these conditions have been determined as being optimal conditions for the process of

the invention that allows the process of the invention to achieve the objectives of the invention.

5. The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Hsu et al (US 5,663,578), Bronner et al. (US 5,792,703) Para et al. (US 5,731,242), Lin (US 5,668,065) and Tai et al. (US 5,851,890) have been examined and have been found to be of general interest to the invention. These prior art records however do not teach the extent and the detail combined with the flexibility of the present patent application.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-26 be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

The invention teaches a new method of filling spacings between high-aspect ration interconnect wiring lines without the formation of non-uniform depositions (such as key-holes) between the interconnect wiring lines. Applicant respectfully submits that the invention teaches methods and processes that in their aggregate are unrelated in design and processing steps of previous procedures and processes.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 914-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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